Fully integrated Sigma-Delta Synthesizer Suitable for "Indirect VCO modulation" in 2.5G application

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Abstract —**A fully integrated ΣΔ fractional Synthesizer (included VCO, Loop Filter, Xtal oscillator negative impedance) is implemented in a 0.4 um, 45 GHz (SiGe) BiCMOS. The measured close in phase noise is -106 dBc/Hz at 900 MHz using 26 MHz comparison frequency and frequency resolution less than 5Hz is achieved. The VCO's inductors are not integrated in order to test the PLL performance on different frequency's range. Using a 200 KHz close loop bandwidth the level of the tones generated, when critical channels are synthesized, exceed the GSM transmitter specifications without applying any dithering technique. The very low close in phase noise and low level of tone generation, make it suitable for "indirect GMSK VCO modulation" application**

I. INTRODUCTION

The 2G and 2.5G standards are becoming more cost sensitive and solutions that reduce the external component count and the number of analog building blocks (A/D converters, VCOs) are fundamental. From this perspective the receiver section has found a mature architecture in the zero IF receiver [1,2,10] that drastically reduce the component count without impacting the selectivity and sensitivity of the system. By the other end the TX section is moving forward to find its optimum solution on the way of the single chip. In this paper we are presenting a state of the art completely integrated SD frequency synthesizer. It is the basic building block of a compact TX architecture that features direct modulation of the synthesizer through the PLL feedback path and able to fulfill the tougher GSM/GPRS specifications (phase noise, settling time, spur).

II. ARCHITECTURE

The proposed architecture (fig1) has been already reported in previous papers [3,4]. The major reported issue of this architecture is the PLL loop parameters' variations; the variations have in fact a great impact on the modulation distortion and on the phase error of the modulated signal. In [3] the issue is not solved but some suggestion are given. In [5] the problem is solved with an extra automatic control system based on a digital phase-locked loop that corrects the modulation error introduced by the main analog narrow band SD PLL. The proposed architecture solves the problem utilizing a digital pre-emphasis filter, it is calibrated to compensate the variation of the open loop PLL DC gain. In the proposed solution the DC gain is the only uncontrolled PLL parameter whose variation's limits are statistically known. The details of the calibration method are disclosed in a patent application which is still pending.

III. TONE GENERATION ANALYSIS

The tone generation in a fractional SD PLL can have different sources:

(a) Phase detector linearity
(b) Idle tone generated by the SD interpolator.
(c) Coupling on die or on board.

(a) It is well known that the commonly used PFD plus charge pump systems have limited linearity. In [6] the author shows that the charge pump is the main contributor to the measured phase noise. Even though there are authors that propose method to solve the charge pump dead zone problem, the impact of the charge pump on the system performance are somehow unpredictable. It has been found (1) that PFD limits the performance of any fractional synthesizer architecture where the fractional spur suppression relies on its linearity. In [9] the fractional tones are suppressed with a dithering of the S-D output paying it with 3 dB higher close in phase Noise.
In our investigation, a PLL matlab model has been developed to show how the dead zone of the PFD (fig. 2) generates spurs on the VCO's output spectrum and makes the sigma-delta high frequency quantization noise fold onto low frequencies (fig. 3).
Based on this consideration the charge pump architecture is abandoned in favor of an Operational Amplifier approach.
Since it is difficult to predict the linearity of the PFD by simulation, but is known [9] that the problem arises close

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to the zero phase error, in the final implementation a programmable leakage current source is connected to the PLL loop filter to offset the PFD bias point and forcing the PFD to work on only one side of its characteristic.

(b) The SD interpolator architecture is based on the one used in [8] and reported in fig.4. The main advantage of this architecture is that it has a limited output swing, limiting the PFD operative point excursion when it is used in a PLL, thus helping to avoid spur tones generation.

(c) There are not accurate methods to predict the coupling among the different sections of a system on chip, but the sources are known by experience and a careful design and layout can help to prevent it.

In the PLL, special care has to be taken in the design of the programmable divider. Because of the lower phase-noise floor [7], the CMOS logic is used for this section. The fast rise and fall time of the rail-to-rail output signal swing generates huge peaks of current flowing on the supply lines. The supply lines act as antennas that radiate on sensitive blocks (VCO for instance). This effect is more important if higher comparison frequency is used.

In this design, the PLL works at comparison frequency of 26 MHz, to overcome the problem the standard pulse swallow architecture divider is abandoned in favor of a four stage 2/3 ECL prescaler followed by a 5 bit CMOS programmable counter. In this way a continuous division ratio from 20 to 128 is obtained and when a 2 GHz frequency is synthesized the CMOS section will work at only 60 MHz.

IV. EXPERIMENTAL RESULTS

A prototype SD fractional synthesizer was fabricated in 0.4-um SiGe BiCMOS technology. The die photo is reported in Fig.4. Fig 5 and fig.6 report the synthesizer phase noise when the SD modulator is enabled and disabled respectively. The SD modulator does not corrupt the close in phase noise of the synthesizer; it shows its contribution at 1MHz where the quantization noise starts to be comparable to the PLL phase noise.

To see the fractional spur performance, a 400 KHz and 200 KHz offset frequency is given from the integer multiple of the phase detector frequency, the output spectra are reported in Fig.8 and Fig.9 respectively. As a result, in the first case a –73 dBc fractional spur at 400 KHz offset is observed, in the second case there are a -60 dBc and a -72 dBc fractional spur at 200 KHz and 400 KHz offset respectively. The loop BW used for the measurements is the same shown by the Phase-Noise plots (fig. 5,6). The reference frequency is generated on the board using the integrated negative impedance and a 26 MHz Quartz. The ΔΣ modulator runs at 2.7V consuming 2 mA. The complete PLL consumes 10mA (crystal oscillator included) and the VCO 35mA (it is meant to meet the GSM TX specification). The VCO gives 6dBm output power.

The Fig. 10 reports the settling time plot where the PLL settles to the wanted frequency (control voltage 2V) starting from the unlocked condition (control voltage 0V).

V. CONCLUSION

A fully integrated high performance fractional frequency synthesizer has been implemented in a standard SiGe BiCMOS process. The measurement data shows that the device can benchmark with the more sophisticate and expensive instrumentation synthesizer where each component is designed and built custom in the more appropriate technology.

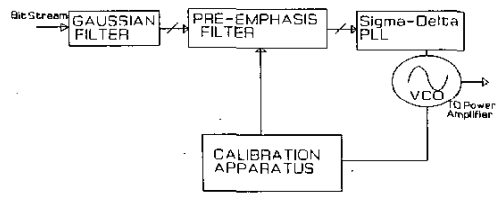

Fig.1: Indirect VCO GMSK Modulation Scheme

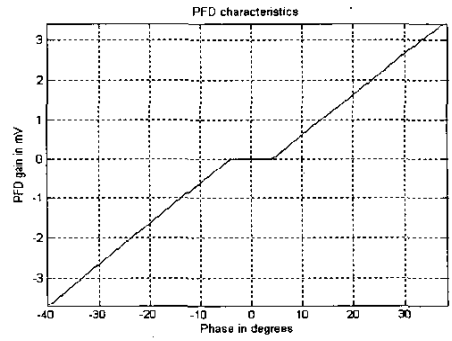

Fig2 . PFD Matlab Model , voltage Vs Phase

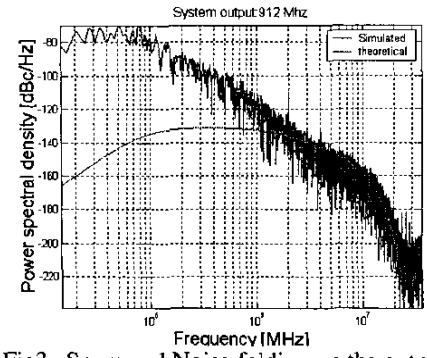

Fig3 . Spurs and Noise folding on the output spectrum

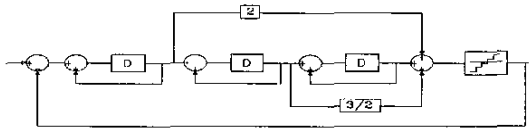

Fig4: Third order SD modulator scheme

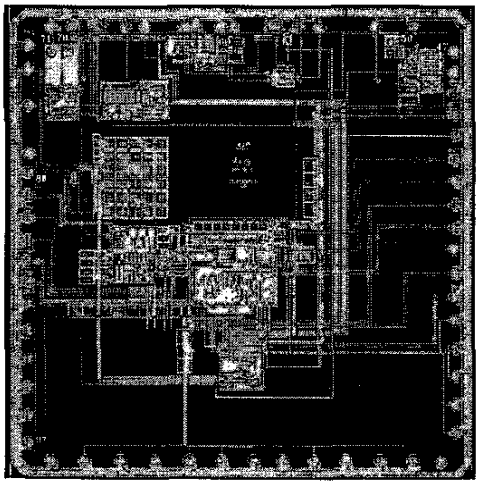

Fig5 : Die photograph

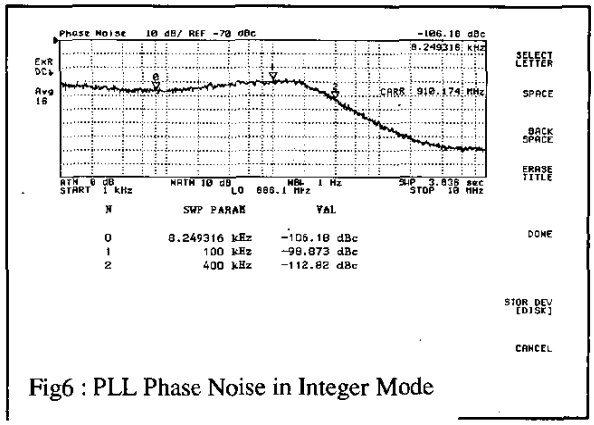

Fig6 : PLL Phase Noise in Integer Mode

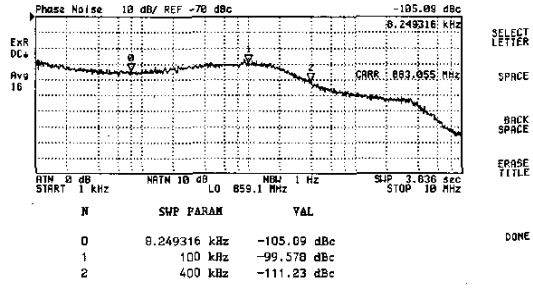

Fig.7: PLL Phase Noise in Fractional Mode

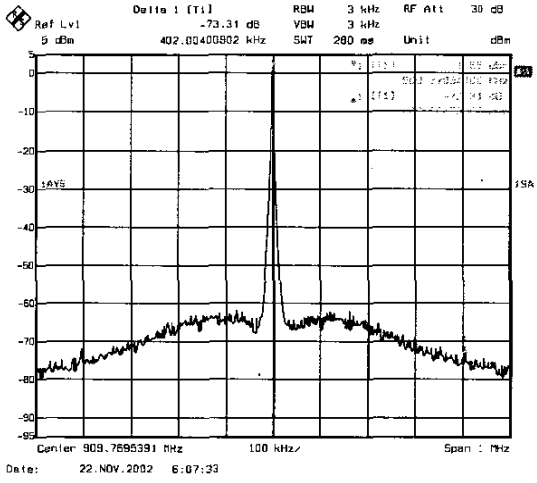

Fig.8: Output Spectrum @ 400 KHz offset from the integer multiple of the phase detector frequency

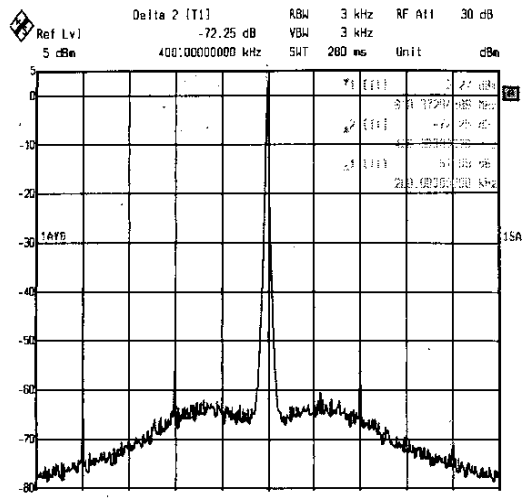

Fig9: Output Spectrum @ 200 KHz offset from the integer multiple of the phase detector frequency

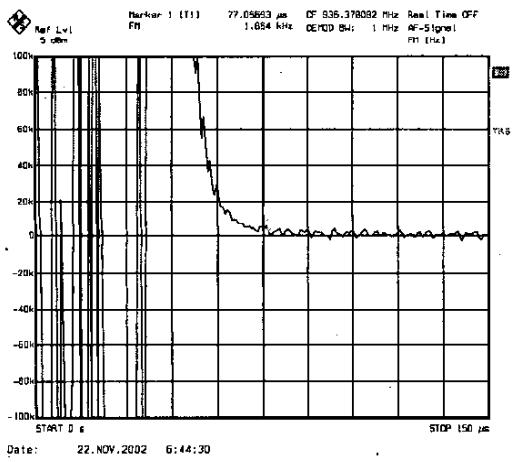

Fig.10: PLL settling time for the VCO control voltage that goes from 0V (unlocked) to 2.2.V

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